when a seventh positive voltage is applied to said buried diffusion region;

an eighth positive voltage is applied to said control gate of a cell to be read;

a ground potential is applied to a bit line connected to the diffusion region closer to a storage node to be read in said cell; and

a ninth positive voltage is applied to the selected word line electrode,

cell data is read with the buried diffusion region as the drain side.

19. The semiconductor memory device according to claim 22, wherein,

when a ground potential is applied to said buried diffusion region;

an eighth voltage is applied to said control gate of a cell to be read;

a seventh positive voltage is applied to the bit line connecting to the diffusion region closer to a storage node to be read in said cell; and

a ninth positive voltage is applied to the selected word line electrode,

a cell data is read with said buried diffusion region as the source side.

20. The semiconductor memory device according to claim 15, wherein the control gate electrode of a cell adjacent to the selected cell is set to a ground potential.